



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/863,030	05/22/2001	Dan F. Ammar	26962	7280

7590 11/05/2003

RICHARD K. WARTHER
Allen, Dyer, Doppelt, Milbrath & Gilchrist, P.A.
P.O. Box 3791
Orlando, FL 32802-3791

EXAMINER

MONDT, JOHANNES P

ART UNIT	PAPER NUMBER
----------	--------------

2826

DATE MAILED: 11/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/863,030	AMMAR, DAN F.	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 July 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-26 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input checked="" type="checkbox"/> Interview Summary (PTO-413) Paper No(s). <u>10/28/3</u> . |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 07/22/03 has been entered.

Response to Amendment

Proposed Amendment After Final Rejection filed 06/30/03 under 37 C.F.R. 1.116 and accompanied by Affidavit under 37 C.F.R. 1.132 has been entered following aforementioned Request for Continued Examination. Simultaneously with said Affidavit all claims have been substantially amended. Comments on said Affidavit and on the Remarks included in said Amendment are offered below under "Response to Arguments".

Response to Arguments

2. Applicant's arguments filed 07/22/03 have been fully considered together with the Affidavit under 37 C.F.R. 1.132: they are persuasive to the extent that the rejections based primarily on Chan et al (5,451,818) no longer can be applied to the newly amended claim language, because Chan et al indeed nowhere suggests or teaches the multilayer thick film substrate board for mm wave transceiver modules formed

constituted of planar sheets of low temperature transfer tape or ceramic material stacked together to form a single, planar substrate board having a planar bottom surface and planar top surface on which planar top surface a plurality of MMIC chips, or even one MMIC chip is mounted, because the MMIC chip 30a is, or MMIC chips 30a and 30b are, attached to different segments of (possibly ceramic) layer 31 on said base plate, or on said base plate, rather than on ceramic multi-layer substrate board 20 (see, e.g., column 3, lines 33-38).

However, as is evident from Hung et al (5,982,250), low temperature co-fired ceramic materials have not only been used below 10 GHz but also for the regime of between 20 and 100 GHz (cf. column 3, lines 43-46), which appears to run counter to section 7 on page 3 of said Affidavit. In fact, despite the substantial amendments to the claim language, claims 16-26 are found to be unpatentable over Hung et al in view of art (Lampen et al) showing a plurality of MMIC chips on a common ceramic substrate, with occasional other additional references.

Furthermore, substantial inconsistencies are detectable in the current (twice amended) claims, as delineated in rejections under 35 U.S.C. 112, first paragraph, below, with repercussions in the form of an objection to the specification.

Finally, objections to the claim language are included as well.

Specification

The Specification is objected to with regard to section [0080], in which it is stated that the MMIC chips are directly connected to the top surface using solder or epoxy

resin. However, this statement is self-contradictory, because the connection through solder or epoxy is by necessity indirect. Instead, it appears from the specification that the solder abuts both the MMIC chips and the top surface.

Claim Objections

3. ***Claim 1*** is objected to because of the following informalities:

(a) The wording "to form a single, planar substrate board having a planar bottom surface and planar top surface" (lines 6-8) should be replaced by: "so as to constitute a single, planar substrate having one planar bottom sheet with a planar bottom surface and one planar top sheet with a planar top surface";

(b) The wording "to the top surface of the substrate board" (lines 9-10) should be replaced by: "to said one planar top surface";

(c) The wording "at the top surface of the substrate board" (lines 21-22) should be replaced by: "at said one planar top surface";

(d) The wording "over the top surface of the substrate board" (line 26-27) should be replaced by: "over the said one planar top surface".

Appropriate action is required.

4. ***Claim 9*** is objected to because of the following informalities:

The wording "about" should be replaced by "substantially".

Appropriate action is required.

5. ***Claim 10*** is objected to because of the following informalities:

The wording “to form a single, planar substrate board having a planar bottom surface and planar top surface on which a plurality of MMIC chips are mounted” (lines 5-6) should be replaced by: “so as to constitute a single, planar substrate board having one planar bottom surface and one planar top surface”.

Appropriate action is required.

6. **Claim 12** is objected to because of the following informalities:

The wording “layers” (line 2) should be replaced by: “planar sheets”.

Appropriate action is required.

7. **Claim 13** is objected to because of the following informalities:

The wording “layers” (line 2) should be replaced by: “planar sheets”.

Appropriate action is required.

8. **Claim 14** is objected to because of the following informalities:

The wording “layers” (line 2) should be replaced by: “planar sheets”.

Appropriate action is required.

9. **Claim 16** is objected to because of the following informalities:

(a) The wording “to form a single planar substrate board” (lines 7-8) should be replaced by: “so as to constitute a single planar substrate board having one planar bottom sheet with one planar bottom surface and one planar bottom sheet with one planar top surface”;

(b) the wording “said layers” (lines 8-9) should be replaced by: “said planar sheets”;

(c) the wording "on the_top surface" (line 19) should be replaced by: "on said planar top surface";

(d) the wording "connected to said DC signals, ground and capacitors and resistors and operable" (lines 23-26) should be replaced by "connected to said DC tracks and connections, to said ground connections, and to said capacitors and resistors, and operable".

Appropriate action is required.

10. **Claim 17** is objected to because of the following informalities:

The wording "multiple layers" (line 3) should be replaced by "more than one of said planar sheets".

Appropriate action is required.

11. **Claim 19** is objected to because of the following informalities:

The wording "a silver epoxy" (line 3) should be replaced by "silver epoxy".

Appropriate action is required.

12. **Claim 21** is objected to because of the following informalities:

The wording "said layers" (lines 2-3) should be replaced by: "said planar sheets".

Appropriate action is required.

13. **Claim 22** is objected to because of the following informalities:

The wording "said layers" (line 2) should be replaced by: "said planar sheets".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

14. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

15. ***Claims 1-9*** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. Through line 9 of claim 1, the claims contain subject matter not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. In particular, while the Specification teaches that the MMIC chips are connected to the top surface using solder or epoxy resin (cf. section [0080]) and while this connection is characterized by the adverb "directly" also in the Specification, Applicant is reminded that the notion of a direct attachment through another substance is inconsistent and hence cannot be enabled.

16. ***Claims 1-9 and 16-25*** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. Through independent claims 1 and 16 said claims contain subject matter not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. In particular, said single, planar substrate board as claimed must have a planar top surface (line 8 of claim 1 and line 8 of claim

16) comprising a planar sheet (line 20 of claim 1) or sheet (line 16 of claim 16) having cutouts secured at said top surface, which is impossible. It is impossible, because said cutouts destroy the planar character of the top surface.

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

18. ***Claim 10*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Hung et al (5,982,250) in view of Lampen et al (6,175,287 B1) and Miehl et al (5,386,085).

Hung et al teach (cf. Figure 2) a plurality of planar sheets 222/224/226 of Itcc stacked together to form a single, planar substrate board 208 (cf. column 4, lines 44-50) having a planar bottom surface 222 and planar top surface 230 on which a MMIC chip is mounted and operable to transmit and receive mm wavelength signals (amplifier, cf. column 4, lines 13-14), and comprising:

a DC signal layer (any conductive layer within 222-226 other than as excluded in the selection as delineated underneath of layer 226 as the ground layer) formed from a separate sheet and having signal tracks and connections (cf. column 4, lines 46-48);

a ground layer 226 formed from a separate sheet and having ground connections 216 (cf. column 5, lines 35-36); and

a device layer (with top surface 230) (cf. Figure 2 and column 5, lines 31-33) formed from a separate sheet and having capacitors and resistors embedded therein that connect to MMIC chips, because metal 204 and microstrips 112 and 122 form capacitors, while each of microstrips 112 and 118 form resistors (also note capacitor with 124 as dielectric) (cf. column 4, lines 15-25);

Hung et al do not necessarily teach a plurality of MMIC chips to be mounted instead of a single chip. However, as shown by Lampen et al, the advantage of supporting a plurality of MMIC chips 22 and 24 (cf. column 2, lines 51-67, and Figures 1-2) through a common substrate 26 (loc. cit.) has long been recognized within the context of integrated circuits including both amplifier and logic chips (cf. column 1, lines 13-22). *Motivation* to include the teaching by Lampen et al in the invention by Hung et al stems at least from the obvious advantage of higher device density achieved through the use of a common substrate. *Combination* is simply achieved by adding another MMIC chip to the substrate board in Hung et al, i.e., include two MMIC chips 110 therein.

Hung et al do not necessarily teach the plurality of planar sheets to be constituted of low temperature transfer tape (lttt) rather than ltcc (low temperature co-fired ceramic material). However, as is evidenced by the description of prior art in Miehl et al a standard low temperature co-firing process for manufacturing ceramic multilayer circuit boards includes providing a conductive, or an insulating substrate with

a conductive pattern thereon, and then transferring and firing a glass-ceramic tape layer to the surface of the substrate. This tape layer provides both electrical isolation between the substrate and electrical conductors or electronic components, which are subsequently bonded to or mounted on the top surface of the glass-ceramic tape layer. By providing vertical electrical conductors by means of vias in the tape layer prior to firing the tape layer directly on the substrate, good X and Y lateral dimensional stability of the tape material is maintained. In addition, a high quality thick film glass-ceramic electrical interconnect structure is achieved at a relatively low manufacturing cost. Motivation to include the teaching by Miehl et al in the invention by Hung et al is the selection of a time-honored specific method of ltcc that ensures material stability and reduction of cost. Combination of said teaching with said invention is straightforward by adoption of a standard variety among standard ltcc methods.

19. **Claim 11** is rejected under 35 U.S.C. 103(a) as being unpatentable over Hung et al, Lampen et al and Miehl et al as applied to claim 10 above, and further in view of Osika (5,254,941), previously made of record. Neither Hung et al, nor Lampen et al, nor Miehl et al necessarily teach the further limitations of claim 11. However, the use of isolation vias has long been known in the art of providing electrical isolation between active devices, such as are taught to be included in Lampen et al, as is demonstrated by the patent to Osika, who discussed the need to provide electrical isolation of active devices through isolation vias and check said isolation (cf. abstract).

Motivation to include the teaching by Osika is the need for active devices to be able to operate independently. The teaching in this regard by Osika can be easily *combined* by providing isolation trenches in the standard manner as already admitted in Applicant's disclosure, and as is also clear from Osika (cf. column 1, line 21-50). Success in the implementation can therefore reasonably be expected.

20. **Claims 12-14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hung et al, Lampen et al and Miehl et al as applied to claim 10 above, and further in view of Murphy (4,453,142). Although neither Hung et al, nor Lampen et al, nor Miehl et al necessarily teach the further limitations of either claim 12, claim 13, or claim 14, Hung et al refer to Murphy in their background of the invention section (col. 1, lines 65-67 and col. 2, lines 1-6), whilst Murphy teaches a substrate thickness of 5 mil in total. Applicant does not disclose in his Specification why the difference between the thickness of each of said layers as claimed and the constraints on the thickness of each of the layers in Hung et al as considered in the standard range in view of Murphy is critical to the invention. Applicant is reminded that it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

21. **Claim 15** is rejected under 35 U.S.C. 103(a) as being unpatentable over Hung et al, Lampen et al and Miehl et al as applied to claim 10 above, and further in view of Chan et al (5,451,818) previously made of record. Neither Hung et al, nor Lampen et al,

nor Miehl et al necessarily teach the further limitation of claim 15. However, said base plate as taught by Chan et al is formed from a CTE matched material, namely CuW (cf. column 2, lines 21-31). *Motivation* to include the teaching by Chan et al is the reduction of thermal stress that results from the selection of a CTE matched material.

Combination of said teaching with said invention by Hung et al c.s. is straightforward because of the invariant ceramic constitution of the substrate board.

22. **Claim 26** is rejected under 35 U.S.C. 103(a) as being unpatentable over Hung et al (5,982,250) in view of Lampen et al (6,175,287 B1).

Hung et al teach a method of forming a thick film mm wave transceiver module comprising the steps of:

a base plate 202 (cf. column 4, lines 41-42);

a thick film, multi-layer substrate board 208 formed by stacking a plurality of planar sheets 222/224/226 (cf. column 4, lines 44-50) of low temperature co-fired ceramic material stacked together to form a single, planar substrate board having a planar bottom surface 222 and a planar top surface 230 on which MMIC chip 110 (cf. column 5, lines 47-61) is mounted and operable to receive and transmit millimeter wavelength RF signals (cf. column 4, lines 13-14), receiving the thick film, multi-layer substrate board on the base plate (cf. Fig., 2 and column 4, lines 44-57), said substrate board comprising:

a DC signal layer (any conductive layer within 222-226 other than as excluded in the selection as delineated underneath of layer 226 as the ground layer) formed from a separate sheet and having signal tracks and connections (cf. column 4, lines 46-48);

a ground layer 226 formed from a separate sheet and having ground connections 216 (cf. column 5, lines 35-36);

a device layer (with top surface 230) (cf. Figure 2 and column 5, lines 31-33) formed from a separate sheet and having capacitors and resistors embedded therein that connect to MMIC chips, because metal 204 and microstrips 112 and 122 form capacitors, while each of microstrips 112 and 118 form resistors (also note capacitor with 124 as dielectric) (cf. column 4, lines 15-25); and
securing the MMIC chips onto the top surface 230 of the thick film, multi-layer substrate board such that the MMIC chip operatively connects to capacitors and resistors embedded within said device layer and other layers via interconnects 232 (cf. column 6, line 9) within the thick film substrate board (cf. Figure 2).

Hung et al do not necessarily teach the further limitation that a plurality of MMIC chips ("MMIC chips" as recited in claim 26) are mounted on said ceramic substrate. However, as shown by Lampen et al, the advantage of supporting a plurality of MMIC chips 22 and 24 (cf. column 2, lines 51-67, and Figures 1-2) through a common substrate 26 (loc. Cit.; N.B. said substrate is cited to be ceramic substrate, see column 2, line 56-58) has long been recognized within the context of integrated circuits including both amplifier and logic chips (cf. column 1, lines 13-22). *Motivation* to include the teaching by Lampen et al in the invention by Hung et al stems at least from the

obvious advantage of higher device density achieved through the use of a common substrate. *Combination* is simply achieved by adding another MMIC chip to the substrate board in Hung et al, i.e., include two MMIC chips 110 therein.


Conclusion

23. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Watanabe et al (5,852,391).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.


NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

JPM
October 28, 2003*